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**Instruction Set Randomization (ISR).** 0x3c. 0011 1100. 0x33. 0011 0011. 0x0F. 0000

11111. Original opcode: Encoding Key: XOR. **New opcode:** ...

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Like the MIPS **instruction-set** architecture, by hardware convention, ..... causes a new

**instruction** word to be read out and a **new opcode** to be sent to the ...

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**instruction-sets.** They tailor the **instruction-set** to the target .... To study the scalability of

the **new opcode-configuration**, ...

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a new category of processors, the dynamic **instruction set** processors (DISPs) ....

**instruction.** Release processor from. HOLD state. Wait **new opcode** ...

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The version of the Mesa **instruction set** under analysis ..... On the other hand, each **new**

**opcode** adds complexity to the implementation. ...

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**Instruction Set Architecture .... Instruction Set Simulator.** Function Libraries ... define a

**new opcode** for byteswap opcode BYTESWAP op2=4'b0000 CUSTO ...

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the ISA (**Instruction Set Architecture**) is specified or not. When the ISA is specified, .... **new**

**opcode** must be unique for a specific application and ...

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**instruction set.** When we write base instructions in patter- .... tions that can be combined

by a **new opcode-combined instruction pattern.** ...

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What is an **instruction set**? An **instruction set** specifies the machine-level (typically binary) .... How could this be specified without a **new opcode**? ...

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Their mechanism requires significant modification to the **instruction set** to ... Memory reference annotation can be implemented by adding a **new opcode** for ...

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**instruction set** may be extended by the addition of up .... These conditions indicate that this cycle is an ARM **instruction fetch** so the **new opcode** ...

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compress a fixed-length **instruction set** and to use a variable-length **instruction set**. Com- ..... information encoded in the head as a **new opcode**. ...

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a **new opcode**. To change the argument, first click on the argument region of the selected ... It's too bad the SimCom **instruction set** ...

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different revisions of the same **instruction set** architecture (ISA), and you certainly don't want to do .... appropriate print method for each **new opcode**. ...

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(writable **instruction set computer**), MISC (minimum **instruction set computer**), ..... **instruction register** sequence out to program memory to get a **new opcode**. ...

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the **new opcode** indicating that the address can be pre- dicted is used, a hardware table is ... **instruction set** modification is minimal while the con- ...  
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We introduced a **new opcode** class RELATIVE2 for these, which differs from. RELATIVE only .... cause its **instruction set** matches very closely the underlying ...  
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